1. (Amended) A display device comprising:

a pair of substrates;

[a liquid crystal material interposed between the pair of substrates;]

an active matrix circuit and a [peripheral] driver circuit provided on one of the pair of the substrates; and

a sealing member formed on said one of the pair of the substrates so as to [seal the liquid crystal material and] cover the [peripheral] driver circuit, the sealing member being capable of light blocking,

wherein said sealing member comprises a pigment for light blocking.

Please add the following new claims.

--2. (New) A display device according to claim 1 wherein the active matrix circuit has pixels arranged in a matrix form, and wherein regions in each of the pixels where source lines and drain lines overlap with a pixel electrode form a black matrix.

3. (New) A display device according to claim 1 wherein one of an electrode or a wiring line connected to a source or drain of a thin-film transistor formed in the active matrix circuit is one of a metal film, a semiconductor film, and a

silicide film, and wherein a light blocking film for the thin-film transistor is formed by using the one of the metal film, the semiconductor film, and the silicide film.

4. (New) A display device according to claim 1 wherein said pair of the substrates are glass substrates or quartz substrates.

5. (New) A display device according to claim 1 wherein said pair of the substrates are bonded to each other with the sealing member.

6. (New) A device according to claim 1 further comprising:

at least a CMOS transistor formed in the driver circuit region, said CMOS transistor having an n-channel thin film transistor and a p-channel thin film transistor;

a thin film transistor formed in each pixel in the active matrix circuit, said thin film transistor having at least an active layer, a gate insulating film adjacent to said active layer, a gate electrode adjacent to said gate insulating film,

wherein a light blocking film is formed over said gate electrode.

7. (New) A device according to claim 1 further comprising a liquid crystal material interposed between the pair of substrates,

wherein said sealing member seals the liquid crystal material.

8. (New) An electronic device comprising:

at least a first substrate and a second substrate;

a driver circuit region formed on said first substrate, said diver circuit region having at least one of a shift register circuit, a NAND circuit, a level shifter circuit or a buffer circuit;

an active matrix region formed on said first substrate, said active matrix region having at least a pixel;

a sealing member formed between said first and second substrates, said sealing member bonding said first and second substrates and covering said driver circuit region; and

wherein said sealing member shields said driver circuit region from light,

wherein said sealing member comprises a pigment for light blocking.

9. (New) A device according to claim 8 wherein said device does not include a black matrix.

10. (New) A device according to claim 8 wherein said shift register circuit comprises at least a clocked inverter and an inverter.

11. (New) A device according to claim 8 further comprising:

at least a CMOS transistor formed in said driver circuit region, said CMOS transistor having an n-channel thin film transistor and a p-channel thin film transistor;

a thin film transistor formed in said pixel, said thin film transistor having at least an active layer, a gate insulating film adjacent to said active layer, a gate electrode adjacent to said gate insulating film,

and further comprising a light blocking film formed over said gate electrode.

12. (New) An electronic device according to claim 8 further comprising image sensing means for constituting a camera wherein an image obtained by said image sensing means is visualized on said liquid crystal device.

13. (New) An electronic device according to claim 8 further comprising a computing means operationally connected to said liquid crystal device.

14. (New) An electronic device according to claim 8 wherein said device is a projector.

15. (New) A device according to claim 8 further comprising a liquid crystal material injected between the first substrate and the second substrate.

16. (New) A display device comprising:

at least a first substrate and a second substrate;

a driver circuit region formed on said first substrate, said diver circuit region having at least a shift register circuit, a NAND circuit, a level shifter circuit or a buffer circuit,

wherein at least a CMOS transistor is formed in said driver circuit region, said CMOS transistor having an n-channel thin film transistor and a first p-channel thin film transistor;

an active matrix region formed on said first substrate, said active matrix region having at least a pixel,

wherein a second p-channel thin film transistor is formed in said pixel;

a sealing member formed between said first and second substrates, said sealing member bonding said first and second substrates and covering said driver circuit region; and

wherein said sealing member comprises a pigment for light blocking and

wherein said sealing member shields said driver circuit region from light.

17. (New) A device according to claim 16 wherein said device does not include a black matrix.

18. (New) A device according to claim 16 wherein said shift register circuit comprises at least a clocked inverter and an inverter.

19. (New) A device according to claim 16 wherein,

said first p-channel thin film transistor comprises,

a first source region and a first drain region formed over said first substrate,

a first channel forming region formed between said first source and drain regions,

a first gate insulating region formed adjacent to said first source and drain regions and said first channel forming region,

a first gate electrode formed adjacent to said first gate insulating film,

said n-channel thin film transistor comprises,

a third source region and a third drain region formed over said first substrate,

a third channel forming region formed between said third source and drain regions,

a third gate insulating region formed adjacent to said third source and drain regions and said third channel forming region,

a third gate electrode formed adjacent to said third gate insulating film,

said second p-channel thin film transistor comprises,

a second source region and a second drain region formed over said first substrate,

a second channel forming region formed between said second source and drain regions,

a second gate insulating region formed adjacent to said second source and drain regions and said second channel forming region,

a second gate electrode formed adjacent to said second gate insulating film,

wherein a light blocking film is formed over said second gate electrode.

20. (New) A device according to claim 19 further comprising: